

Application No.: 09/751,623  
Amendment Date: April 14, 2006  
Reply to Office Action dated: December 14, 2005

### REMARKS/ARGUMENTS

Claims 1-4, 6-13 and 15-24 are pending in the present application. Claims 1-4, 6-13 and 15-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Morrison et al. (Pub. No.: US 2002/0038398) in view of Sarangdhar (US Patent RE 38,388). Claims 1 and 19 are amended to bring them into better form.

Applicants respectfully submit the cited references do not teach suggest or disclose “[a] method for executing a locked bus transaction in a multi-node system, comprising: ...asserting a signal to said bus agent by said first node controller to prevent said bus agent from initiating a bus transaction.” (e.g., as described in the embodiment of claim 1).

The Office Action states Morrison discloses the method further comprising asserting a signal to said bus agent by said first node controller to prevent said bus agent from initiating a bus transaction in paragraph [0028], wherein pending locked transaction means preventing. Applicants respectfully disagree. Paragraph [0028] states:

After controller 106 obtains semaphore 129, it receives from memory 117 de-assertion of a bus priority agent (BPRI) signal 216, which is used by memory controller 117 as an arbitration signal indicating that memory 126 may receive the locked transaction. *In particular, memory 117 asserts BPRI signal 216 when it forwards data from one side of bus 115 to the other (see FIG. 1), and it de-asserts BPRI signal 216 when forwarding queues 104 and 105 are empty, indicating that system 100 is quiesced.* The term quiesced means that the locked transaction may issue on an associated bus required or used for the transaction, and in this example it means bus 115 is clear of pending transactions from other processors and memory 117 may receive the locked transaction. *(emphasis added)*

The only signal disclosed in the Morrison reference is the BPRI signal. The BPRI signal is asserted by the memory 117 when it forwards data from one side of bus 115 to the other, and the memory de-asserts the signal 216 when the forwarding queues are

Application No.: 09/751,623  
Amendment Date: April 14, 2006  
Reply to Office Action dated: December 14, 2005

emptied. However, the Morrison reference does not disclose asserting a signal *to prevent a bus agent from initiating a bus transaction* as described in the embodiment of claim 1.

The Office Action further asserts that Morrison teaches asserting a signal to said bus agent by said first node controller to prevent said bus agent from initiating a bus transaction in that Morrison discloses the IOKILL signal notifying the I/O bridges via a bus to stop issuing transactions because of a pending locked transaction. *See Office Action dated 12/14/2005, page 6, paragraph 4.a. Applicants respectfully disagree.*

In its rejection, the Office Action asserts that Morrison describes transmitting a locked bus request to a first node controller in paragraph [0025]. *See Office Action dated 12/14/2005, page 2, paragraph 3. Paragraph [0025] states:*

*In operation, controller 106 receives a request for a locked transaction from one of the processors 223 and 224 via bus 116 and connection 219. IOQ 209 receives and stores the locked transaction. In response, snoop response generation 210, interacting with IOQ 209, retries the transaction on bus 116 while setting an associated lock number pin. In parallel with retrying it, the transaction is transferred via local control 206 to processor queue 203, which in turn notifies request generate 201. In response, request generate 201 issues an invalidate transaction to a location of a lock\_on address in memory 126 in order to acquire semaphore 129. Once it has acquired semaphore 129, request generate 201 sends a notification that semaphore 129 is acquired through IOQ 202 and quiesce state machine 204 to snoop response generation 210. (emphasis added)*

Therefore, presumably the Office Action equates the “locked transaction” request to controller 106 as the equivalent of “transmitting a locked-bus request to a first node controller” as described in the embodiment of claim 1. Applicants disagree.

However, only for the purposes of this argument, Applicants will assume *arguendo* that this is the case. If the Office Action asserts that controller 106 is the equivalent of the “first node controller”, then the Office Action must show where Morrison teaches the controller 106 asserts a signal to said bus agent to prevent said bus

Application No.: 09/751,623  
Amendment Date: April 14, 2006  
Reply to Office Action dated: December 14, 2005

*agent from initiating a bus transaction* (e.g., similar to that described regarding the first node controller in the embodiment of claim 1). Morrison does not.

As described above, the Office Action asserts that the IOKILL signal is the "equivalent to applicants claimed preventing agent from initiating". See Office Action, page 6, paragraph 4.a. The IOKILL signal is not described in cited paragraphs [0026] or [0028]. The description of the IOKILL signal, found in paragraph [0027], states:

Snoop response generation 210, in parallel with retrying the transaction, also notifies quiesce state machine 204 of the pending locked transaction. *In response, quiesce state machine 204 issues an input/output kill (IOKILL) signal on line 214.* IOKILL signal 214 notifies the I/O bridges within the system, via bus 115, to stop issuing transactions because of a pending locked transaction. When bus 115 is clear of transactions, an input/output acknowledge (IOACK) signal 213 received from other controllers in the system, via bus 115, acknowledges that they have completed issuing their pending transactions. Controller 106 and the controllers in nodes 107-109 may use sideband signals to issue and receive IOKILL signal 213 and IOACK signal 214. (*emphasis added*)

Therefore, the Office Action's cited section describes the IOKILL signal being sent by a quiesce state machine (204), *not* a controller (e.g., 106). In order to support a proper §103(a) rejection, the Morrison reference the equivalent of "*...transmitting a locked-bus request to a first node controller ... and asserting a signal to said bus agent by said first node controller to prevent said bus agent from initiating a bus transaction*" (e.g., as described in claim 1). It does not.

Sarangdhar fails to make up for the deficiencies of Morrison. Although Sarangdhar is directed toward performing bus transactions, it does not disclose asserting a signal *to prevent a bus agent from a bus agent from initiating a bus transaction*.

In order to be a proper 103 (a) rejections, each and every limitation of an claim must be found in the cited references, along with a suggestion or motivation to combine.

Application No.: 09/751,623  
Amendment Date: April 14, 2006  
Reply to Office Action dated: December 14, 2005

Since neither Morrison nor Sarangdhar disclose all of the limitations of independent claim 1, the 103(a) rejection is improper and should be withdrawn. Claims 10, 19 and 21 contain similar allowable limitations. Claims 2-4, 6-9, 11-13, 15-18, 20 and 22-24 are allowable for depending from allowable base claims.

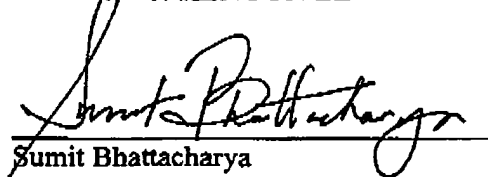
For at least the above reasons, Applicants respectfully submit that the present case is in condition for allowance and respectfully requests that the Examiner issue a notice of allowance.

The Office is hereby authorized to charge any fees determined to be necessary under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Kenyon & Kenyon Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

Respectfully submitted,

KENYON & KENYON LLP



Sumit Bhattacharya  
(Reg. No. 51,469)  
Attorneys for Intel Corporation

Dated: April 14, 2006

KENYON & KENYON LLP  
333 W. San Carlos Street  
Suite 600  
San Jose, CA 95110  
Tel: (408) 975-7500  
Fax: (408) 975-7501